

GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

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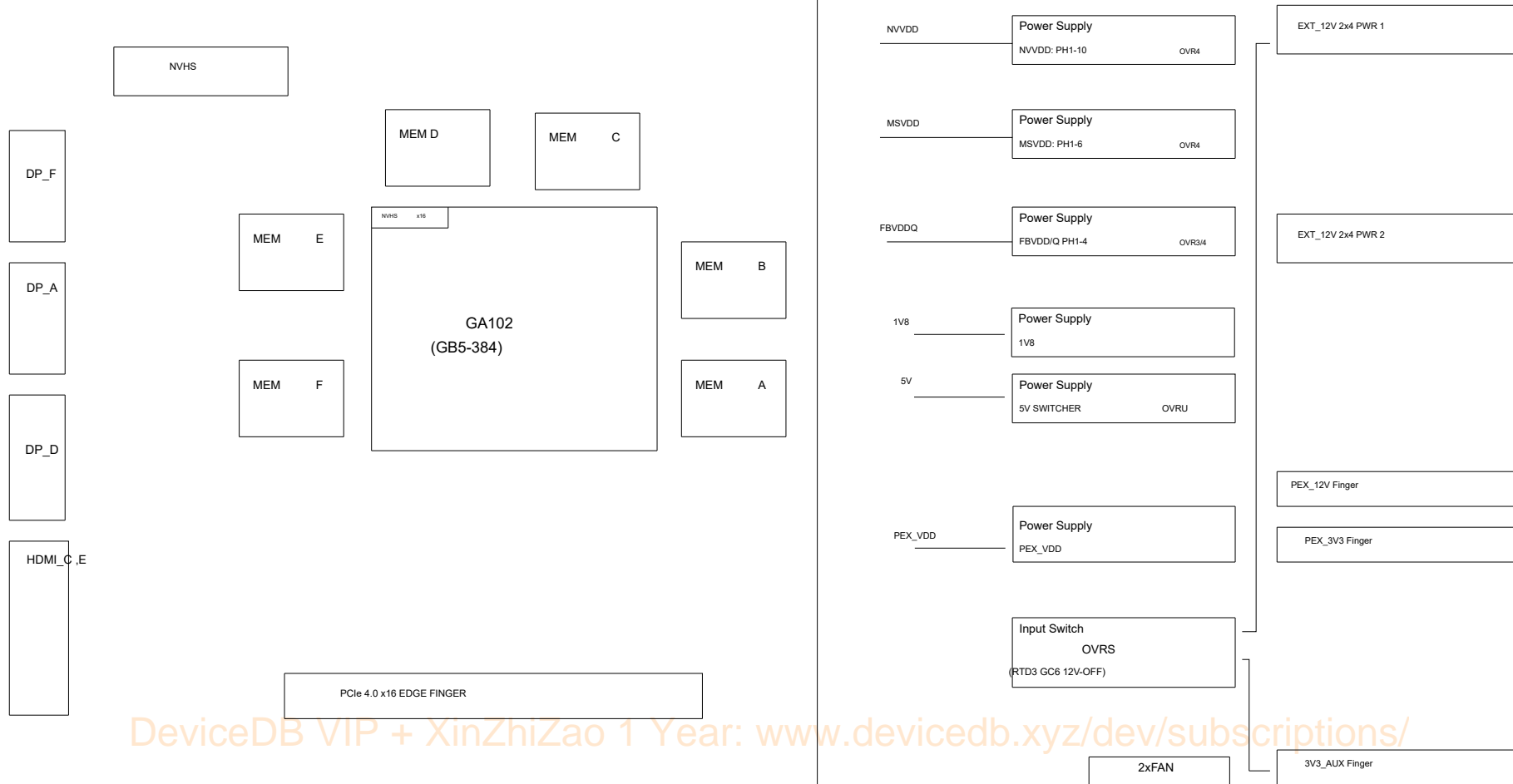
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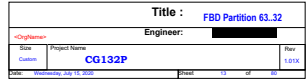
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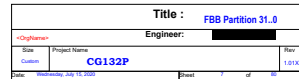
Block Diagram

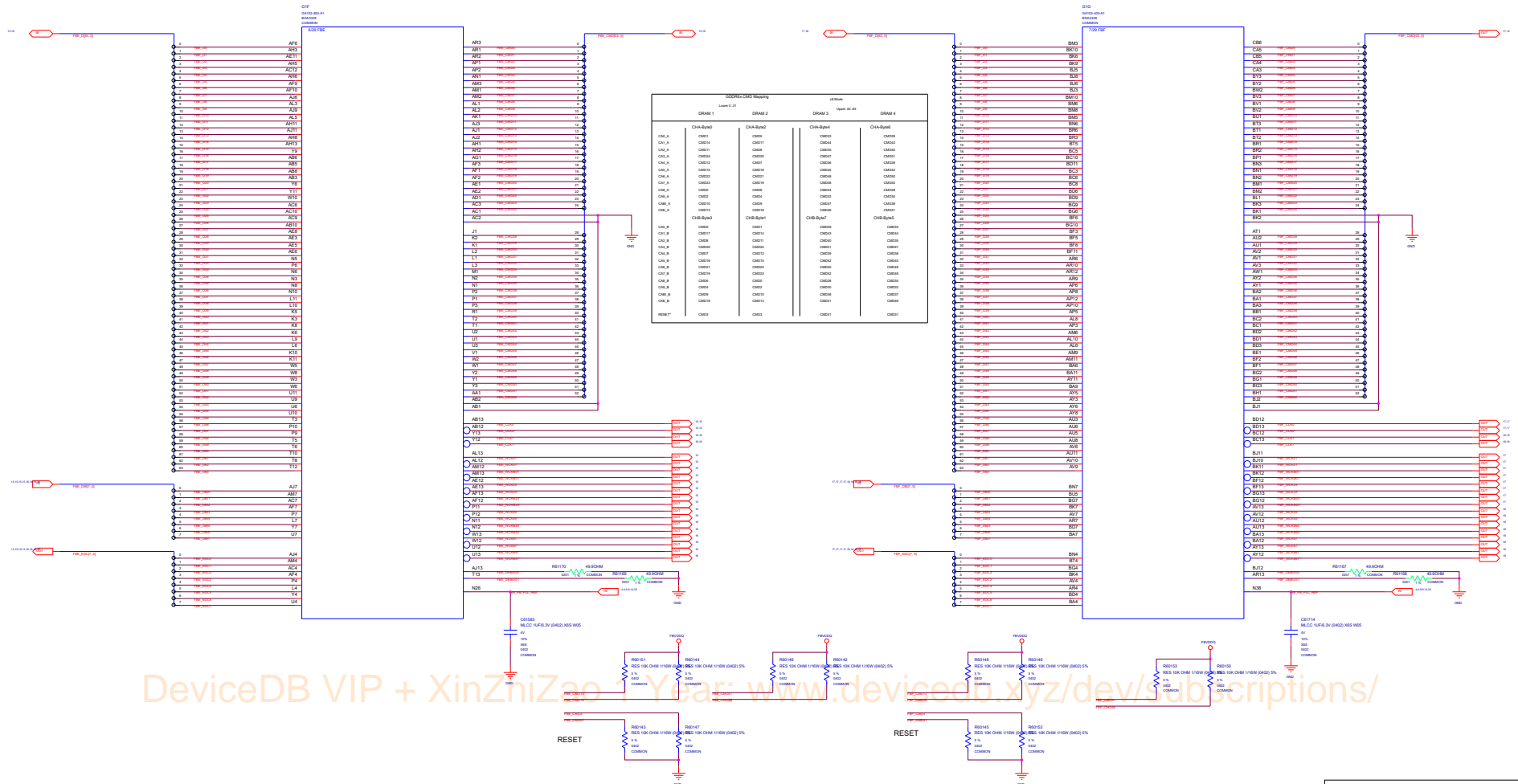


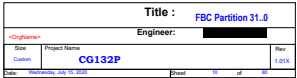
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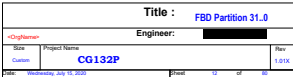
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Engineer:					
<OrigName>					
Size	Project Name			Rev	
Custom	CG132P			1.01A	
Date: Wednesday, July 15, 2009				Phase: 1 of 60	

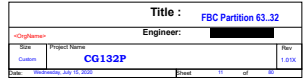


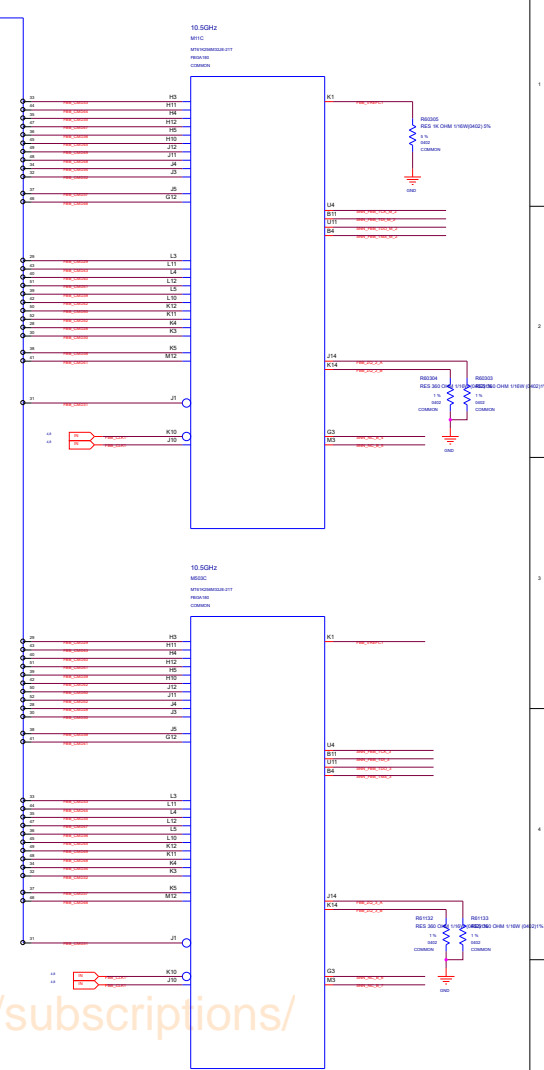
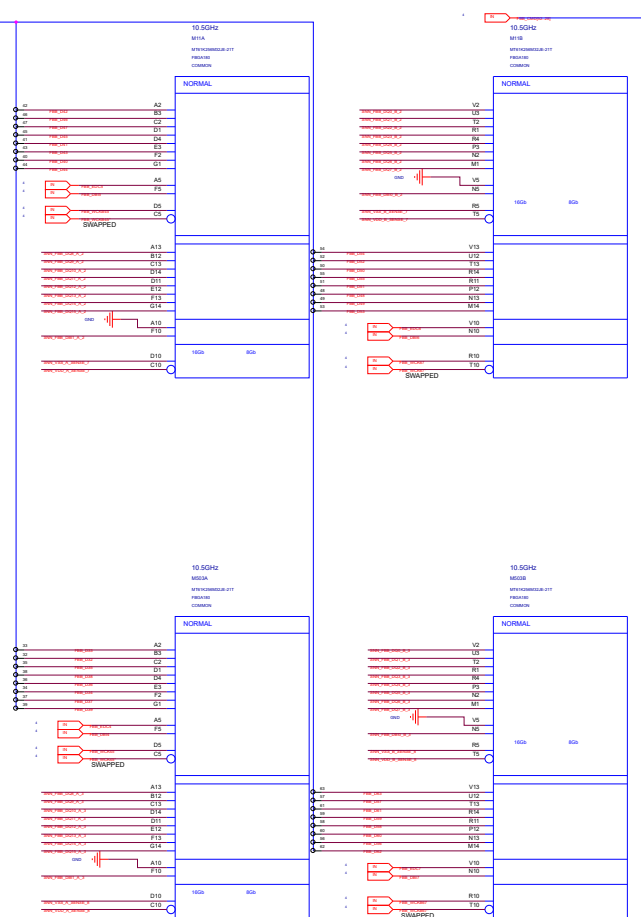


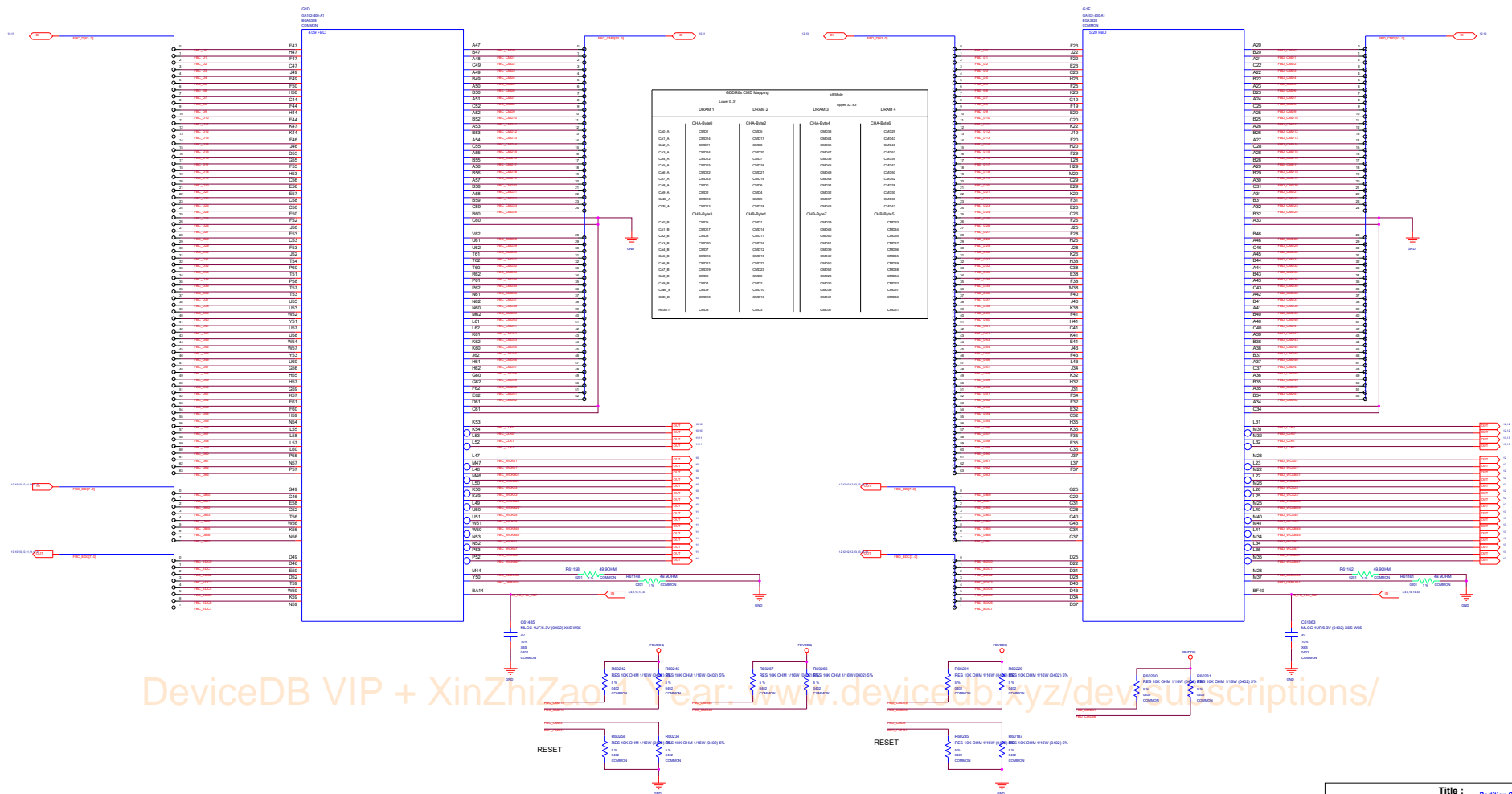


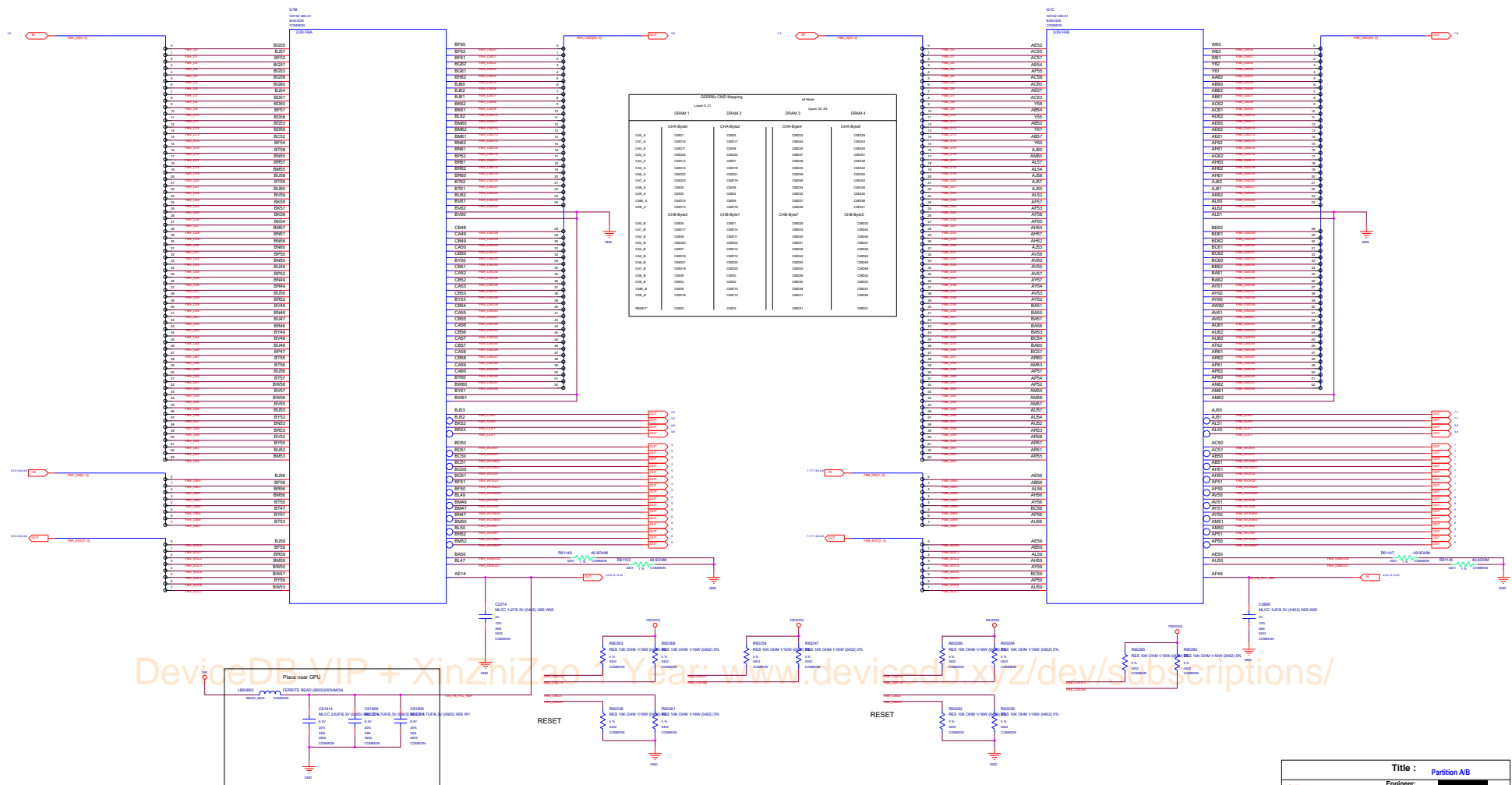




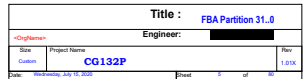


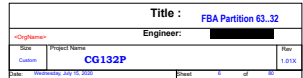
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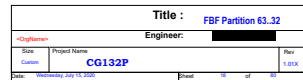
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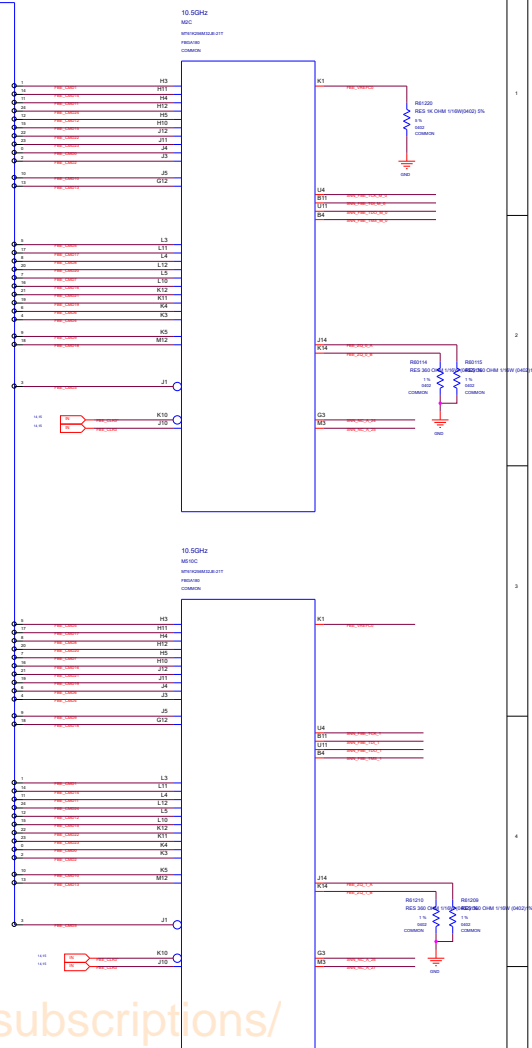
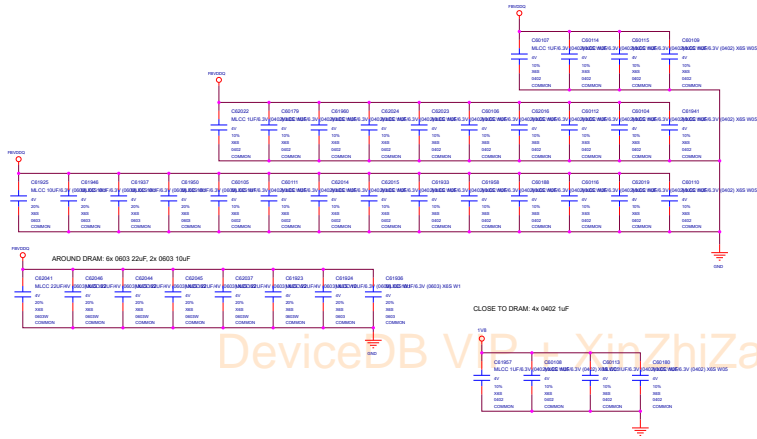


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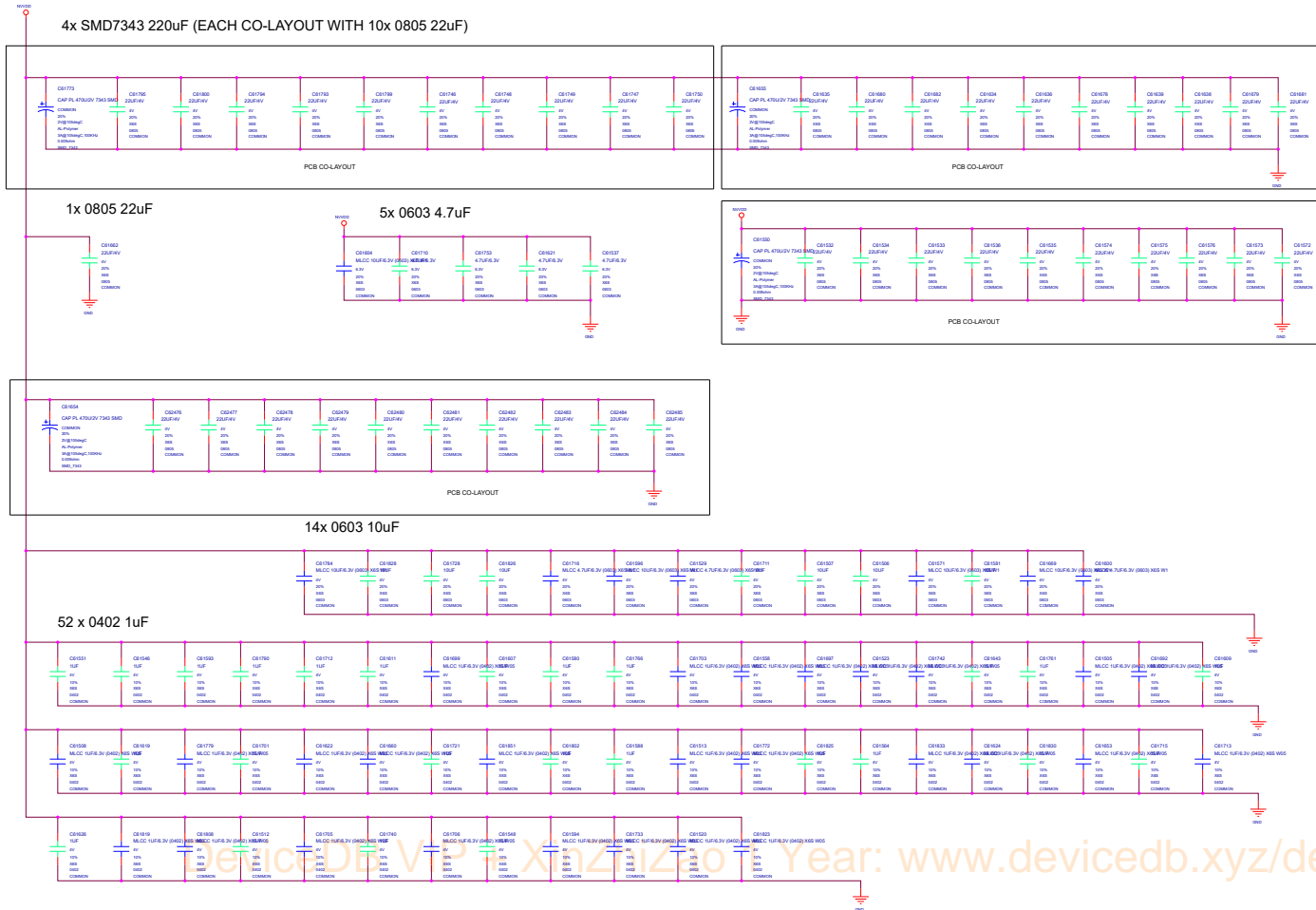


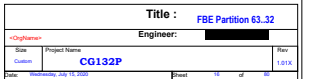


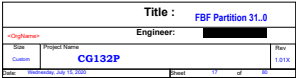




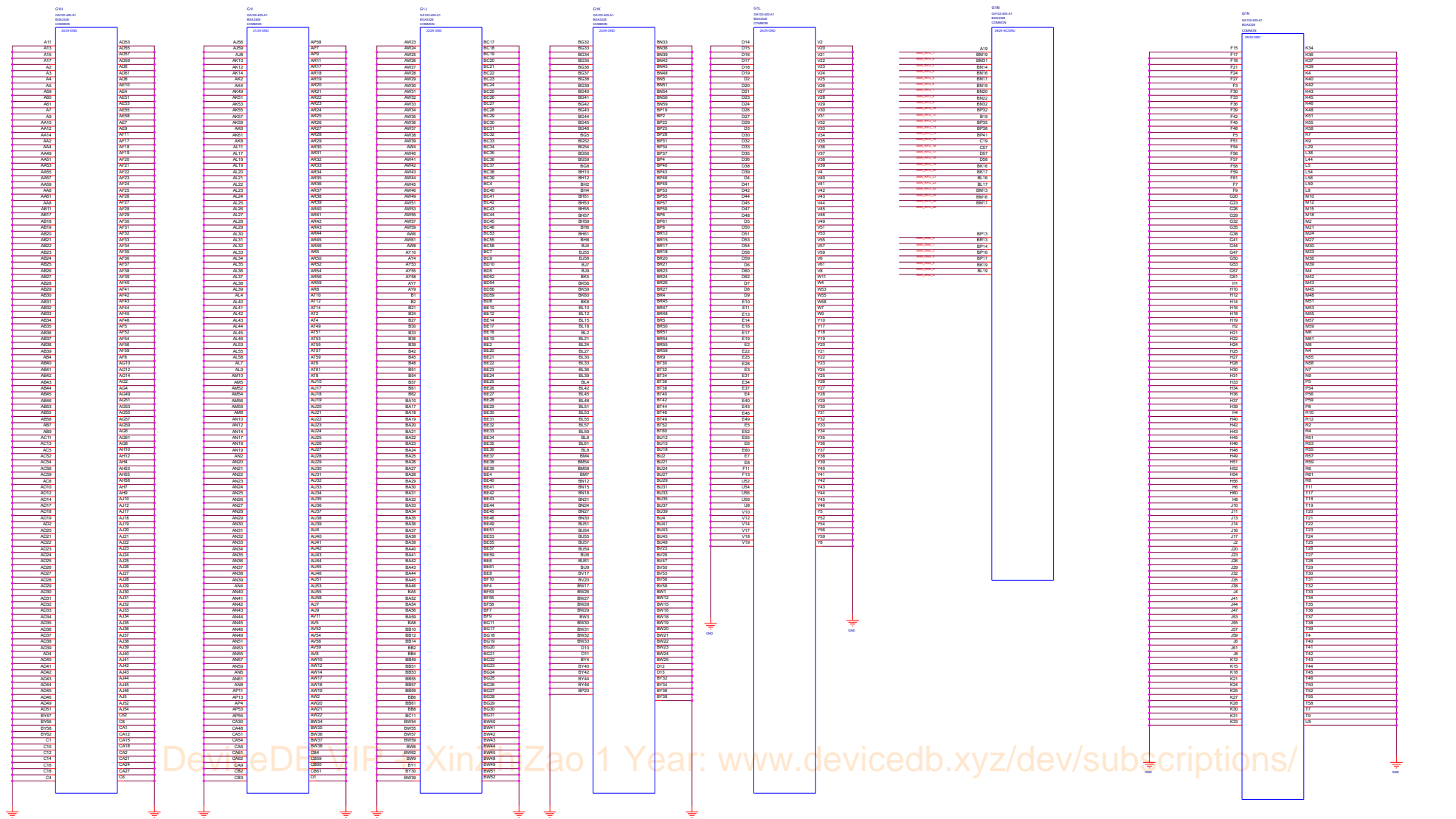
UNDER GPU

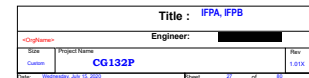




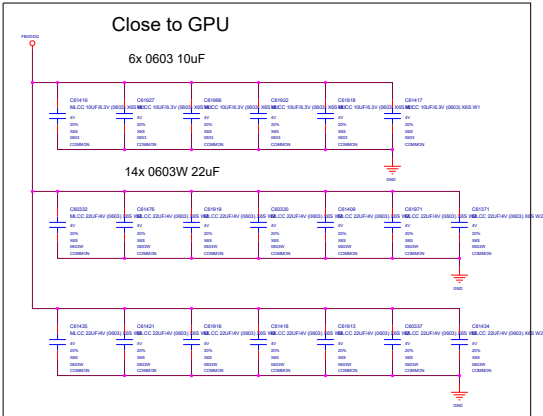
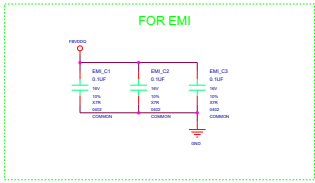
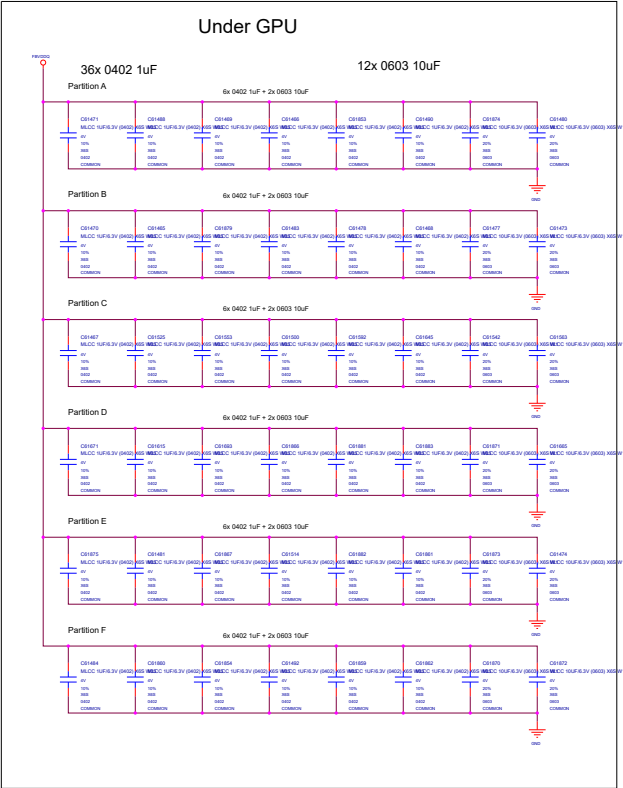


GPU GND, RFUs & RSVD

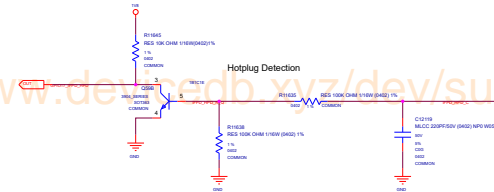
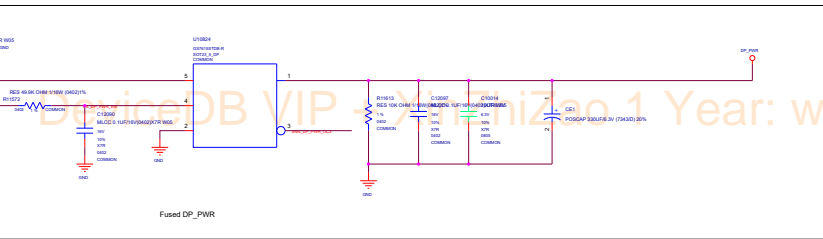
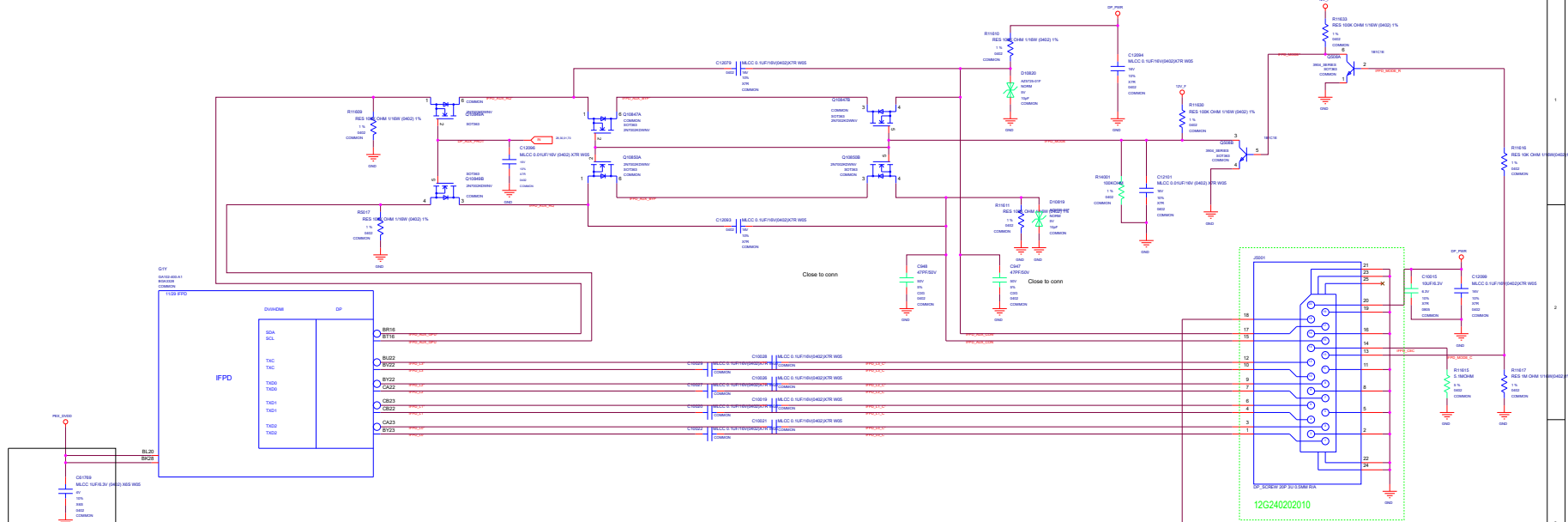




FBVDDQ

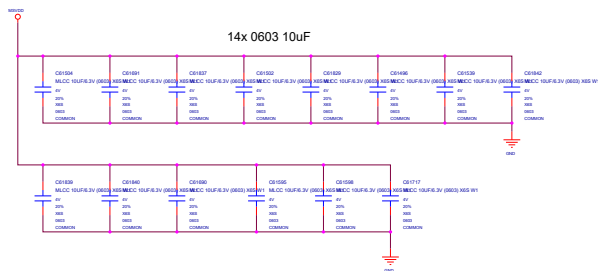


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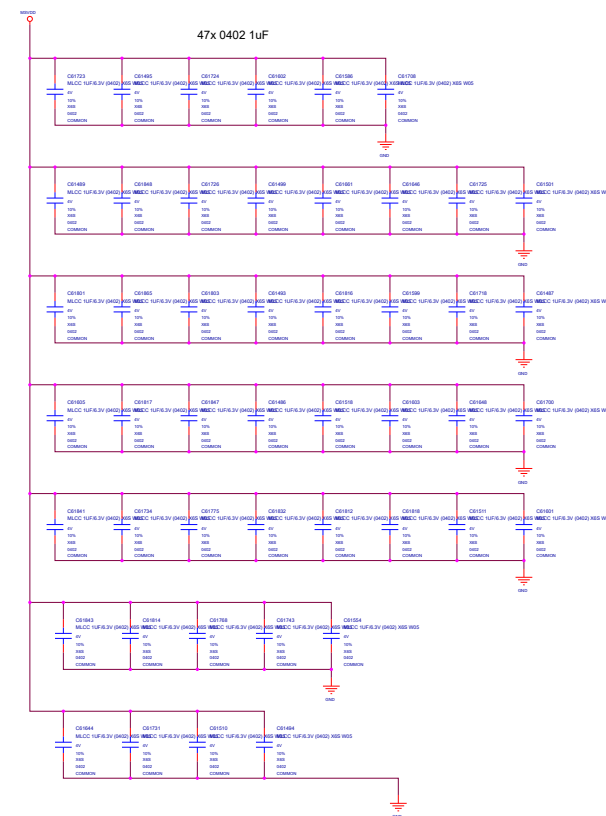


MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

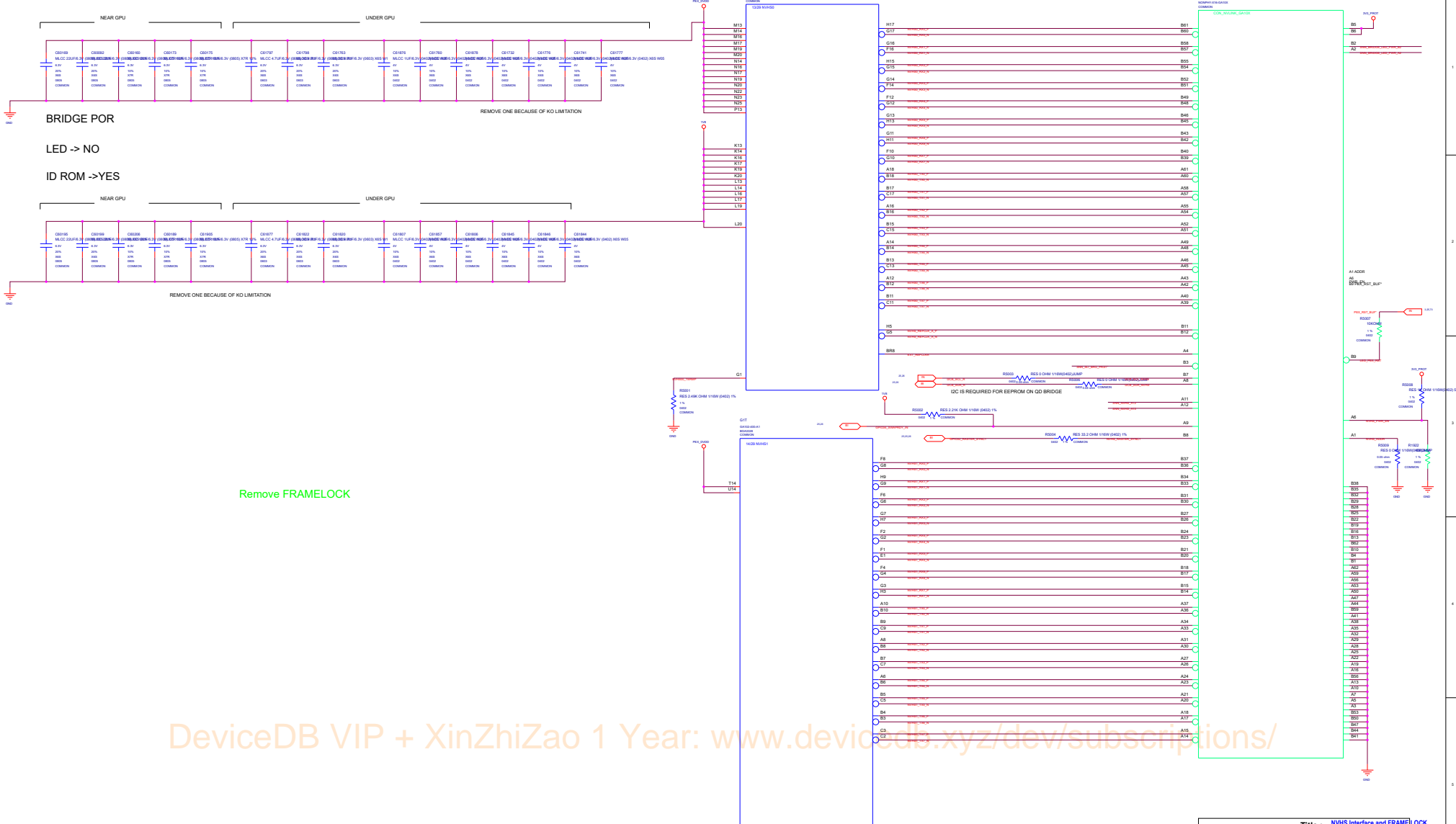
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<OrgName>		Engineer: [REDACTED]	
Size Custom	Project Name CG132P		Rev 1.01
Date: Wednesday, July 15, 2020		Sheet 23 of 80	

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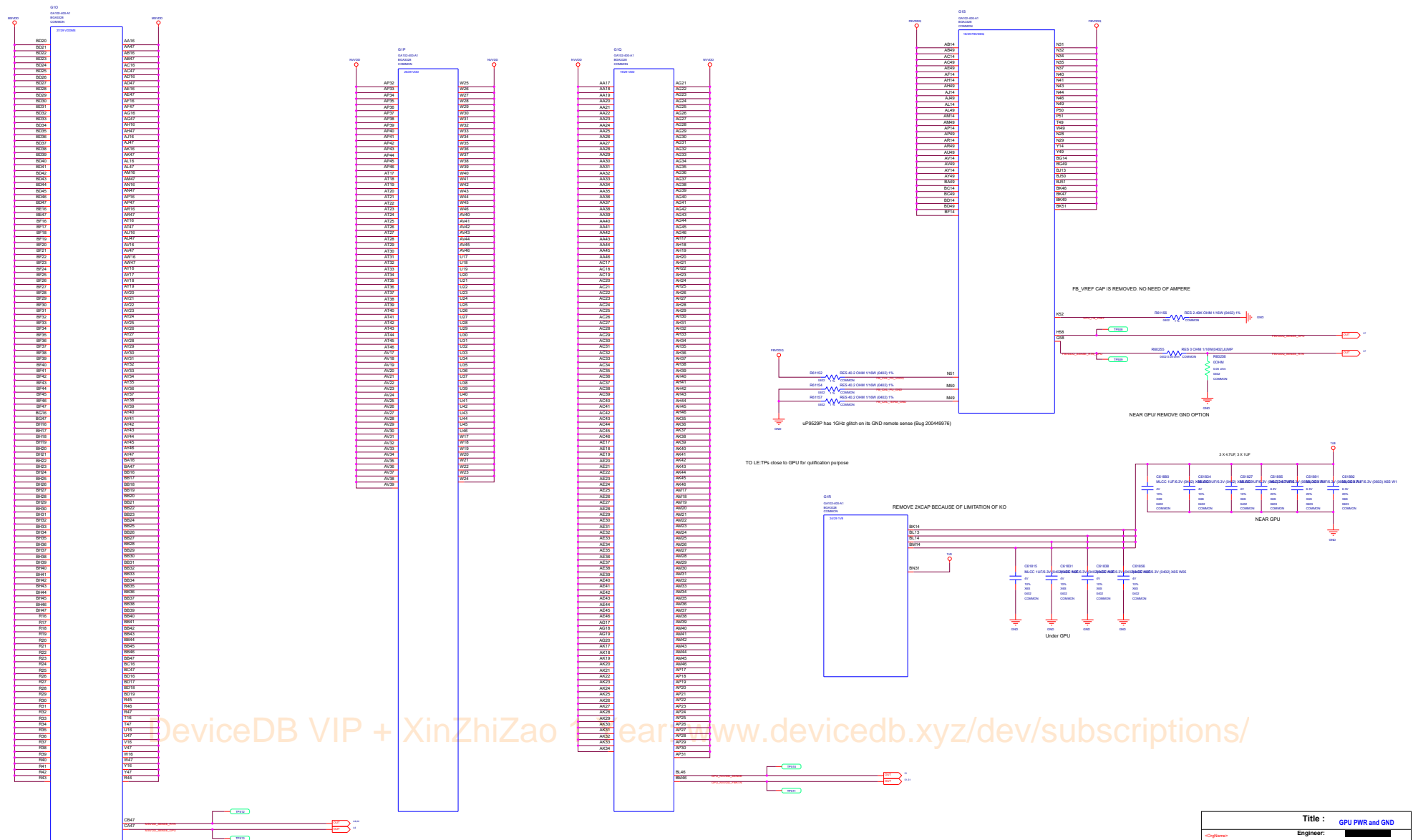
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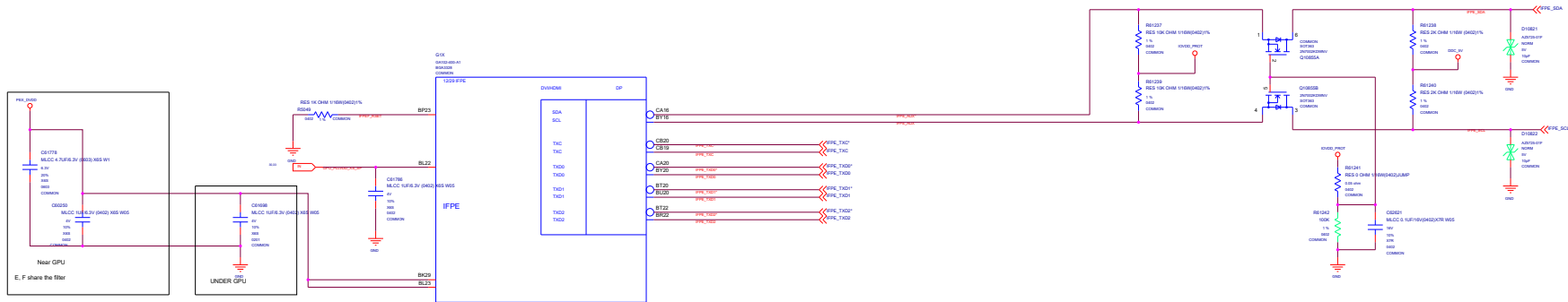
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Engineer:		[REDACTED]	
Drawn	Project Name		Rev
Checked	CG132P		1.0/1X
Date	Wednesday, Aug 14, 2024		Sheet 01 of 01

NVHS Interface and FRAME LOCK

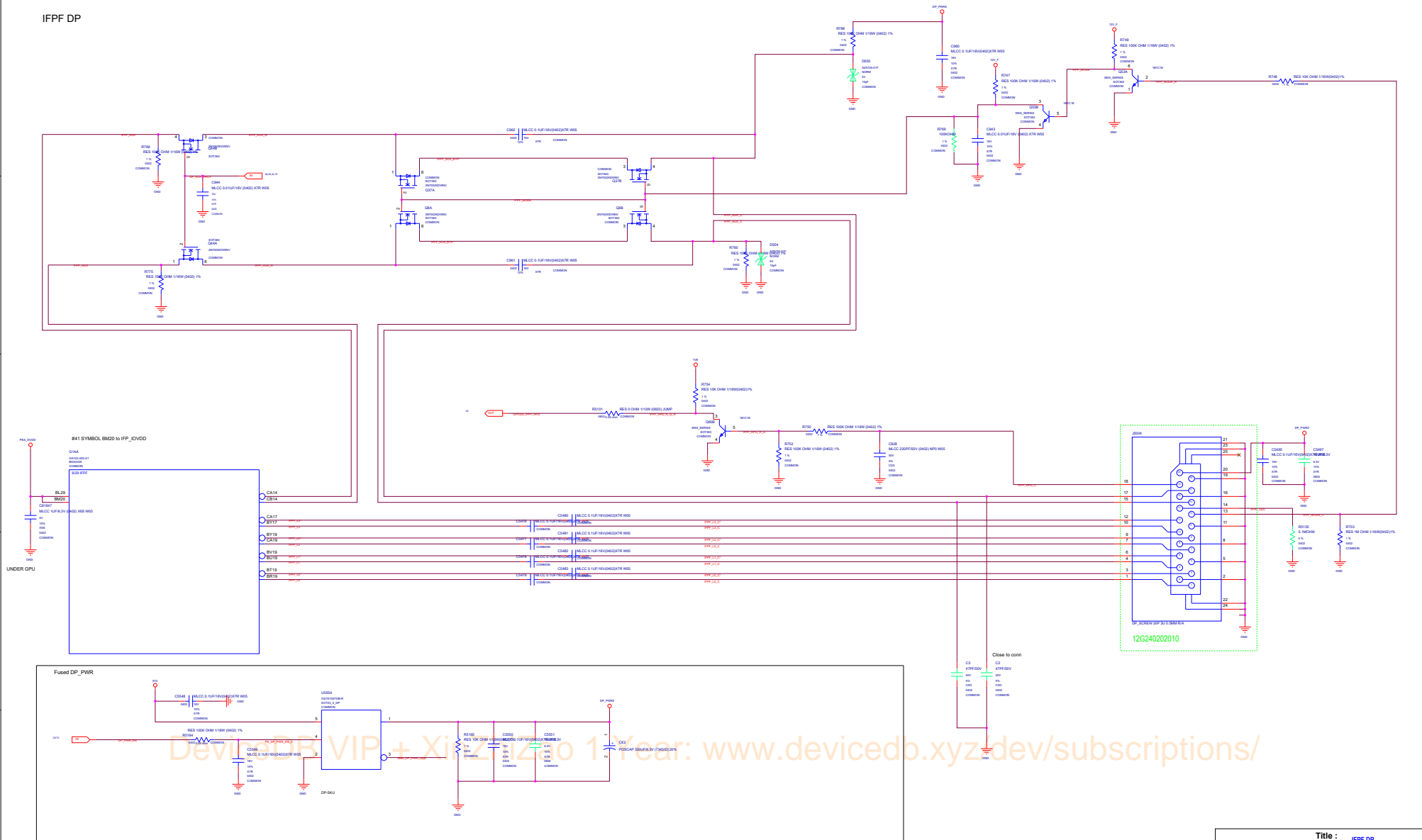


GPU PWR and GND





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MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	0001	RAMCFG TBD
H	L	L	0010	RAMCFG TBD
H	L	H	0011	RAMCFG TBD
H	L	H	0011	RAMCFG MICRON 8Gb 21Gbps

H:High :Tied to 1.8V
M:Middle:Tied to 0.9V
L:Low :Tied to 0V

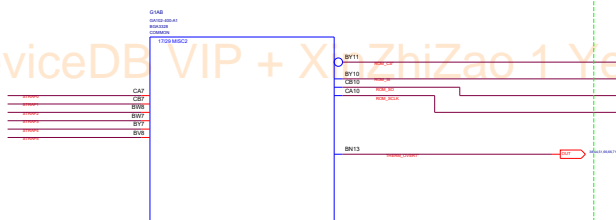
DEFAULT

ROM_SO	ROM_S0	ROM_SCLK	SMARTFAN[2:0]FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

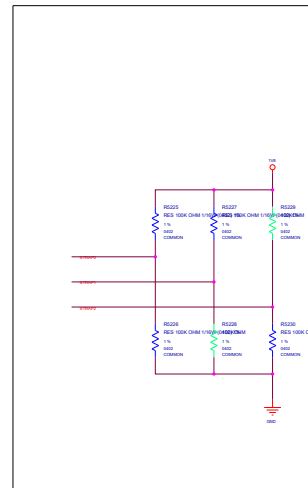
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	0
L	L	H	0	0	1	0
L	L	L	0	0	0	1
L	L	L	0	0	0	0

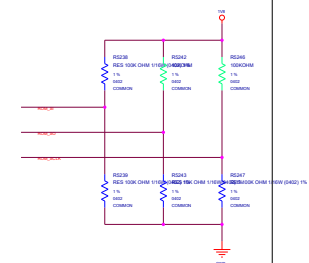
Default



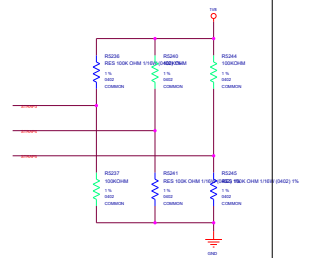
GROUP0



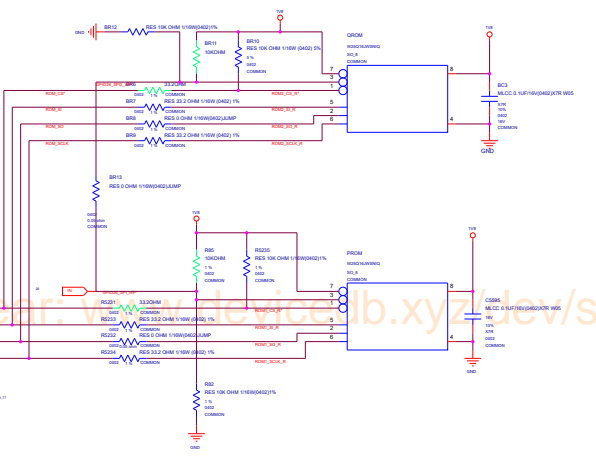
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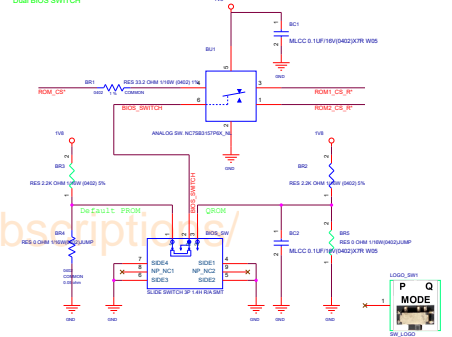
GROUP2



Dual BIOS

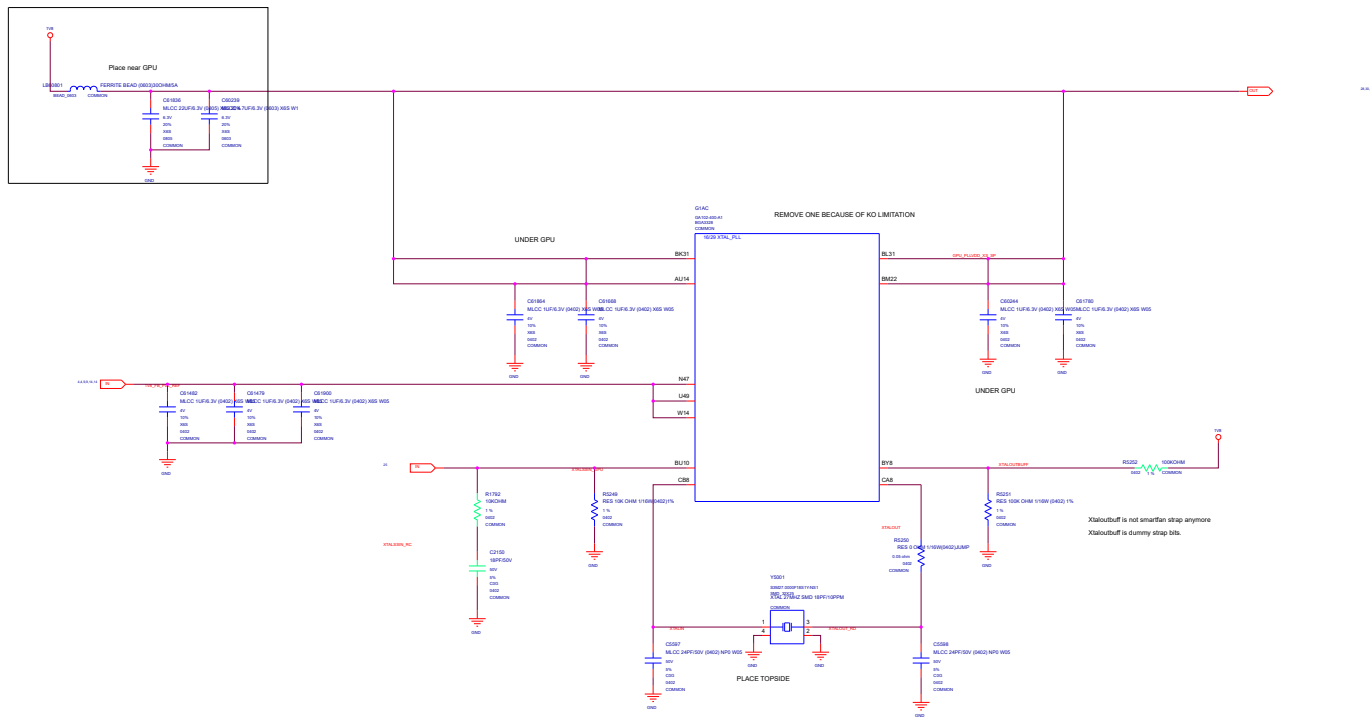


Dual BIOS SWITCH



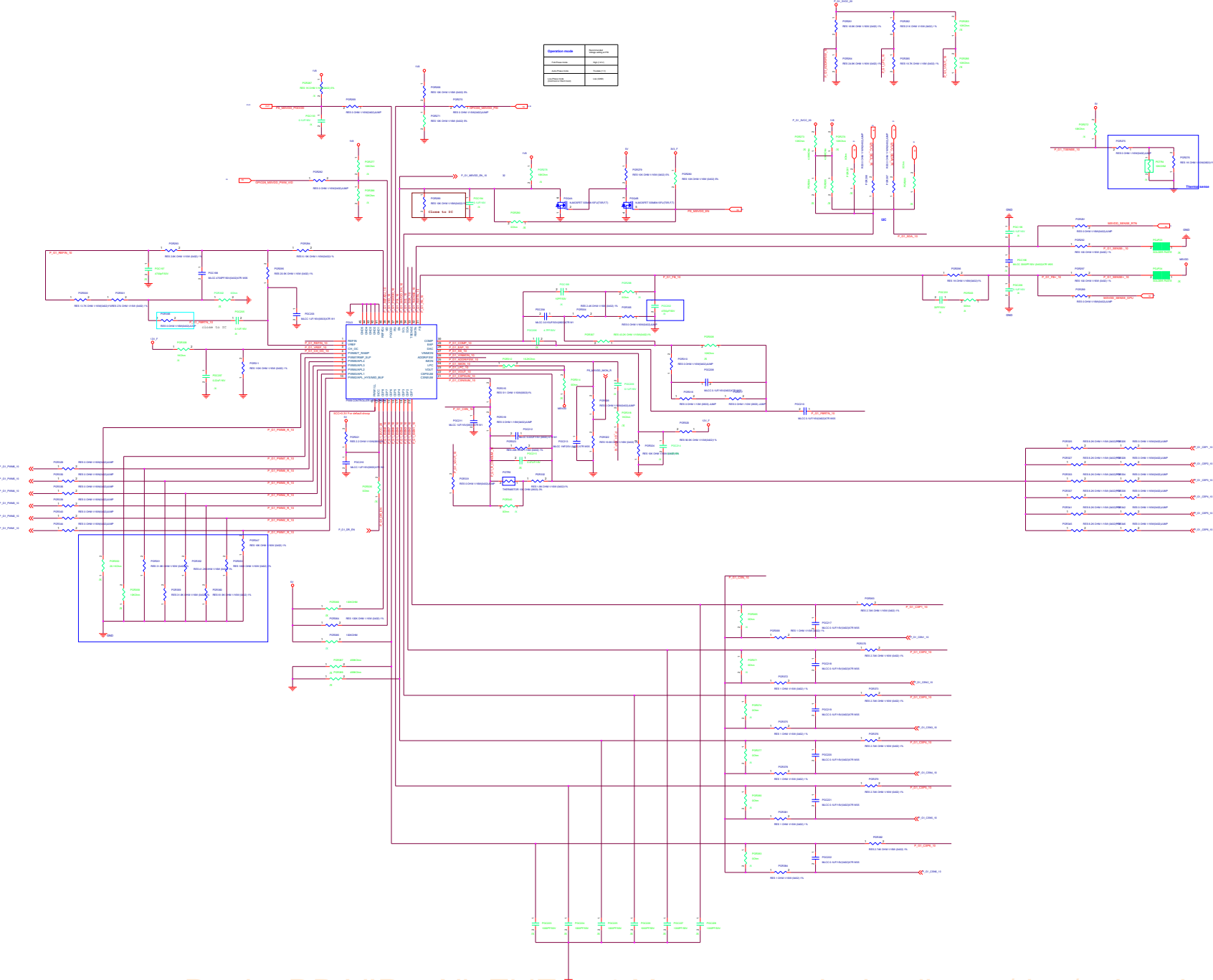
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Version	1.0
Project Name	CG132P
Date	2023/03/10

MISC: XTAL. PLL



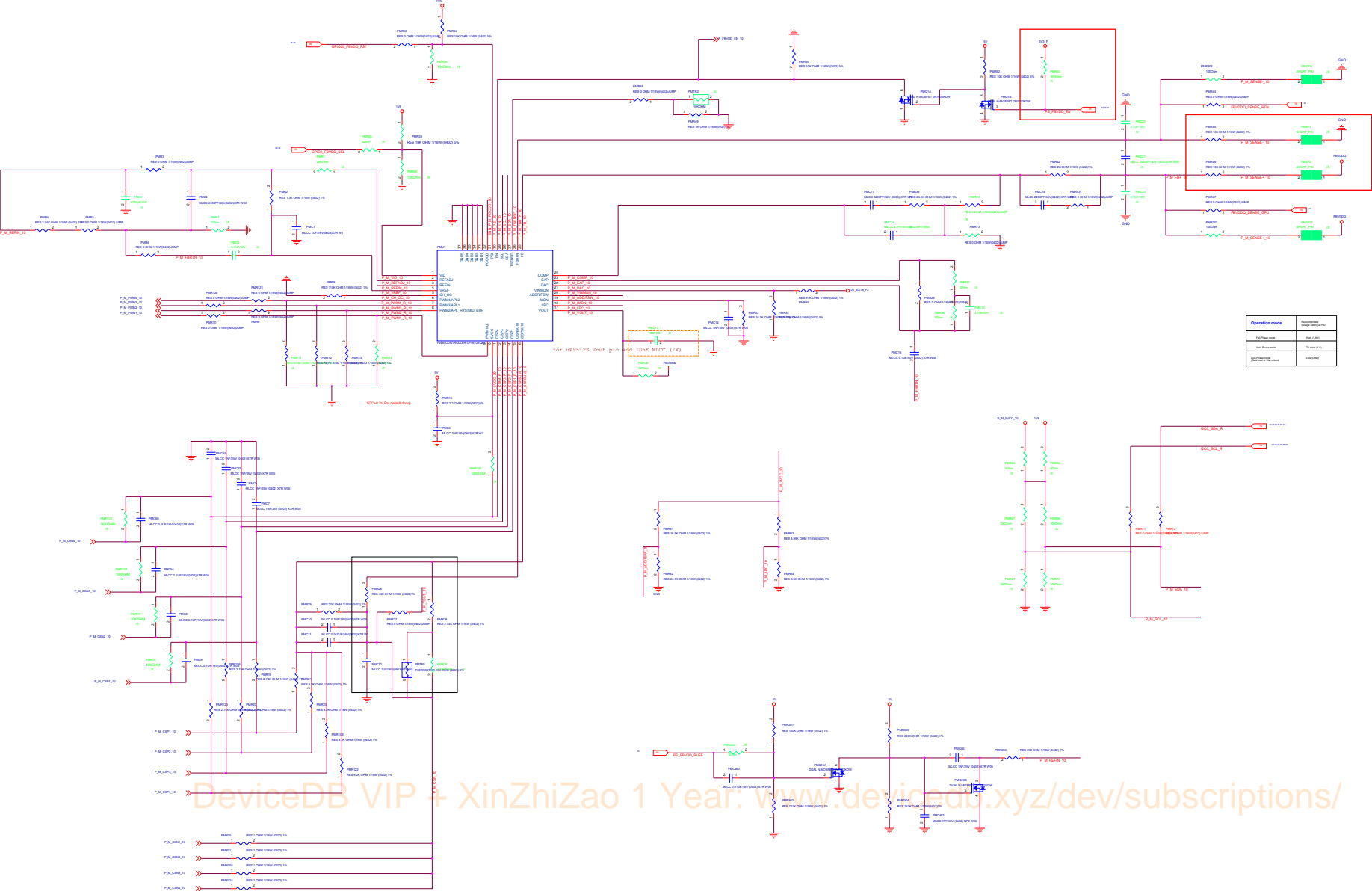
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<OrigName>		Engineer:	
Size	Project Name		Rev
Custom	CG132P		1.0
Date:	Wednesday, July 15, 2003	Sheet	33 of 85

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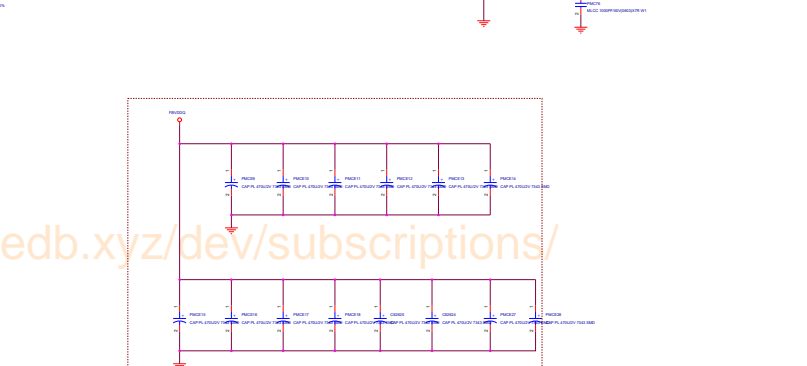
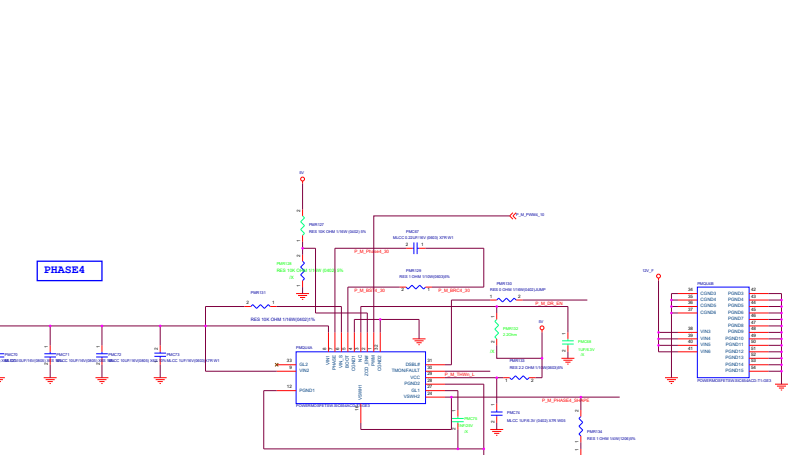
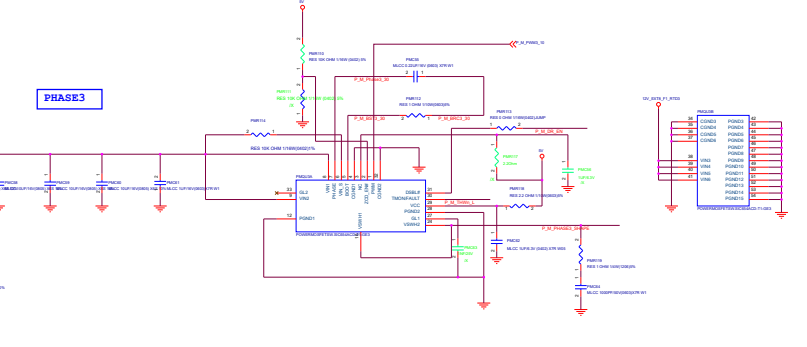


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		Title :		PS: 1V8	
<OrgName>		Engineer:			
Size Custom	Project Name CG132P				Rev 1.01X
Date: Wednesday, July 15, 2020		Sheet		35	of 80



Operation mode	Measurement range (mV)
Auto mode	0.1V
Manual mode	0.1V
Auto mode	0.1V



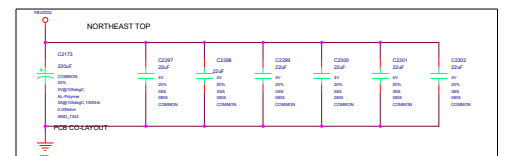
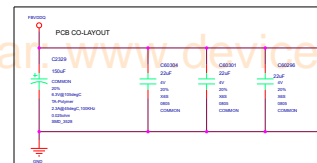
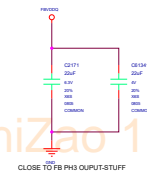
AND GATE LOGIC FOR P-BOARD

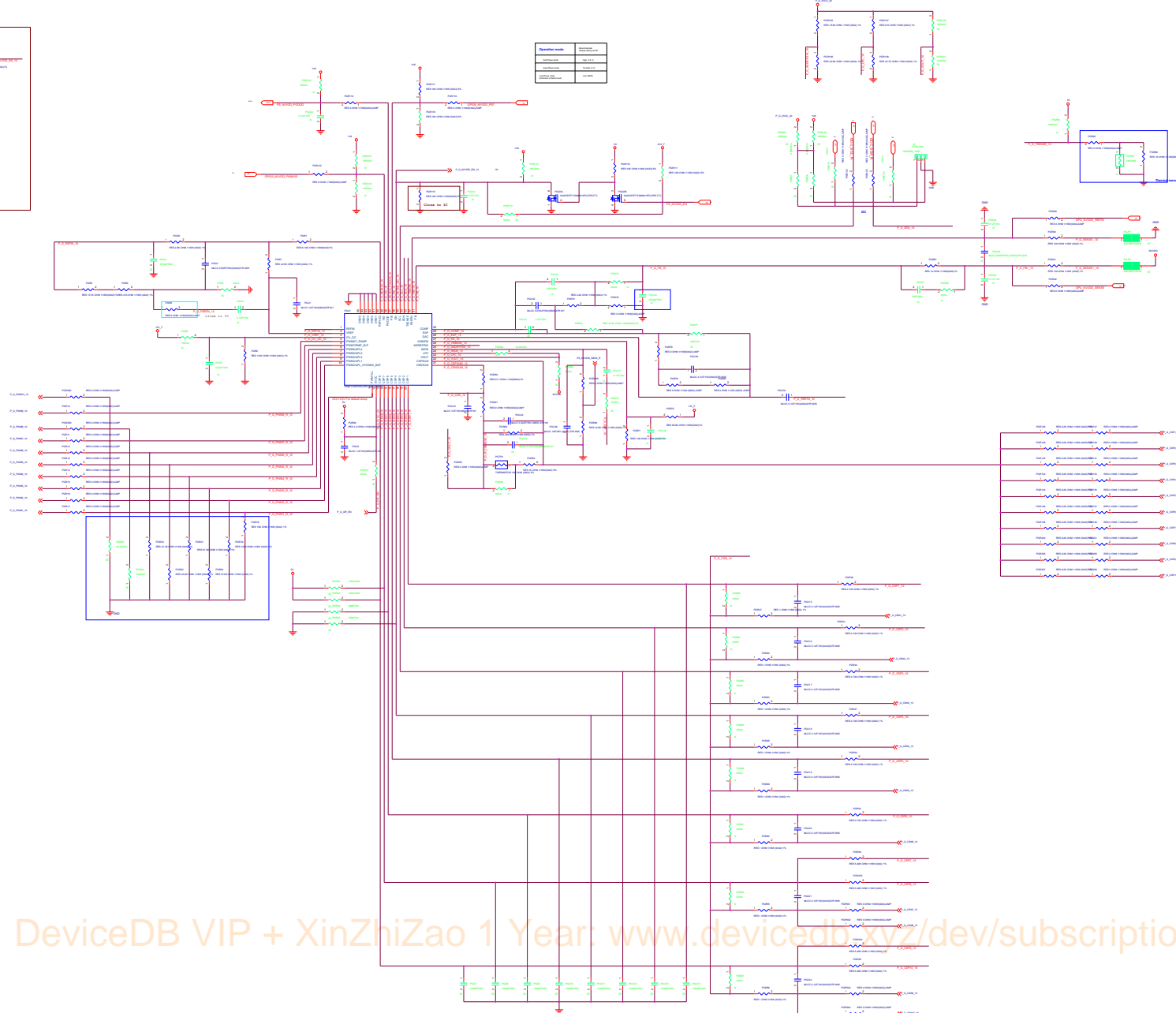
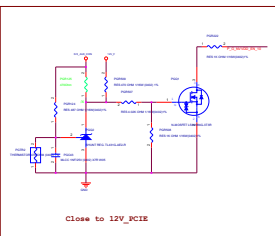
GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



Remove RTD3 Switch Function

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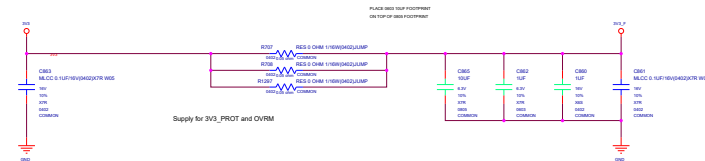




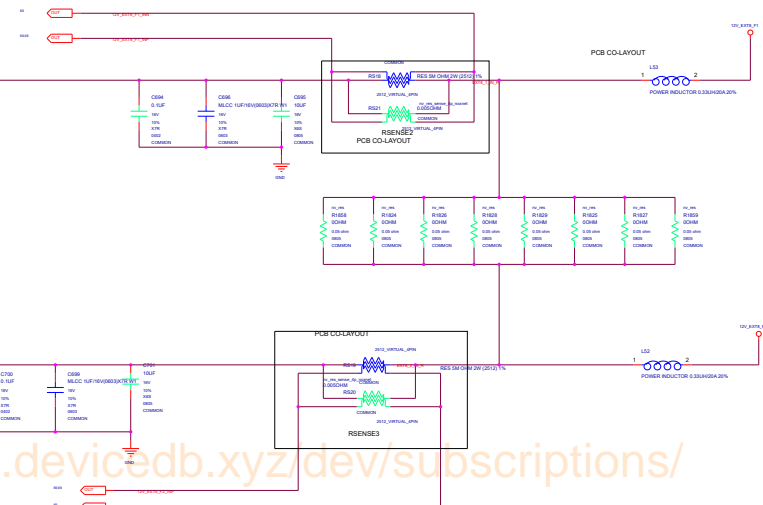
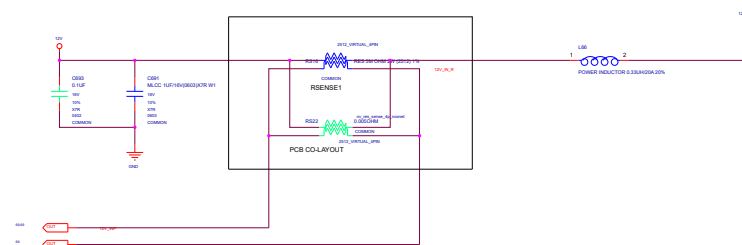
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

Remove 3V3_AUX FUSE

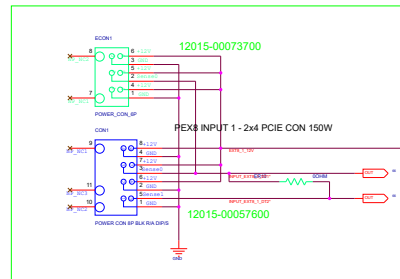
PEX 3V3 INPUT - 10W



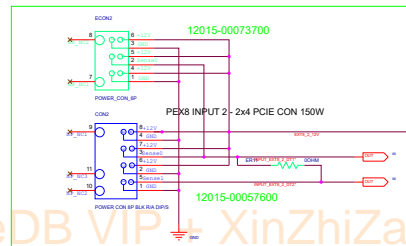
PEX_12V INPUT - 66W



Reverse lock

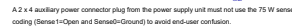


Reverse lock

DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/Remove J24, J25, J26, J27
MECH_SPECIAL_SOLDERING_PIN_LARGE-PG160



Remove Hot-Unplug Detect function



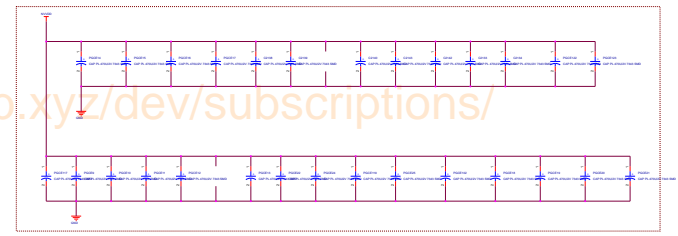
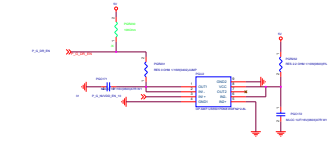
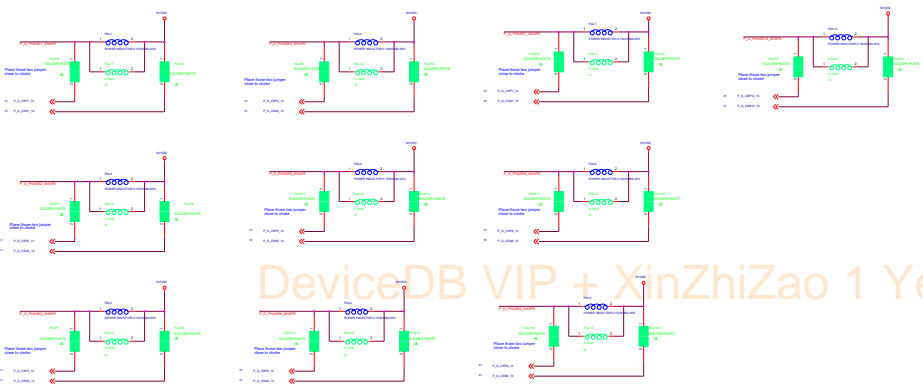
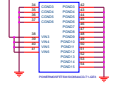
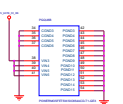
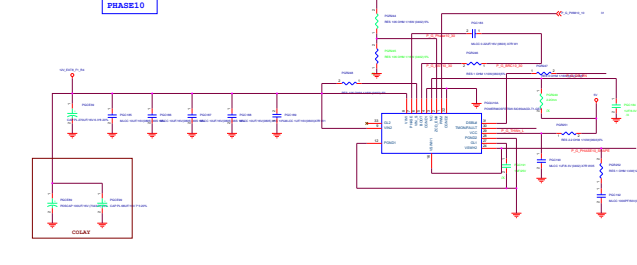
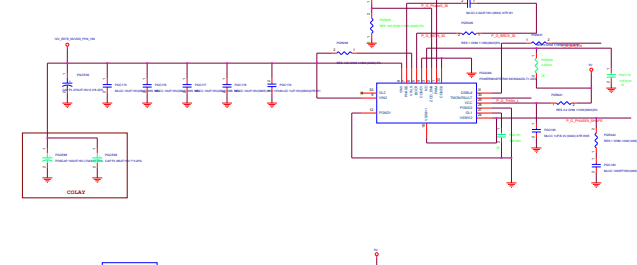
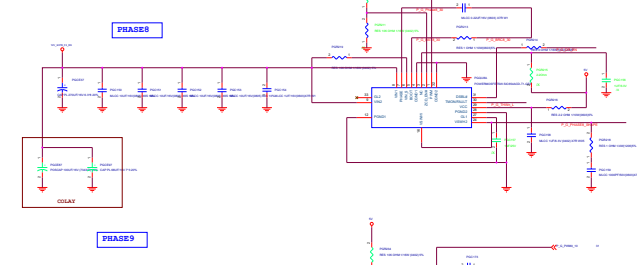
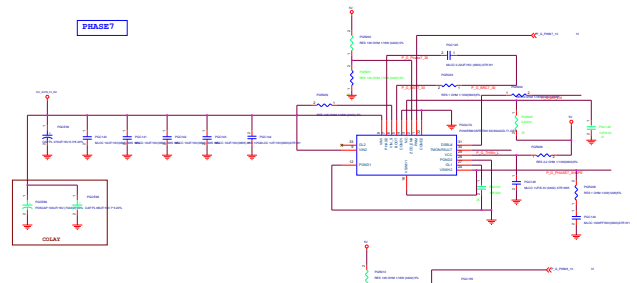
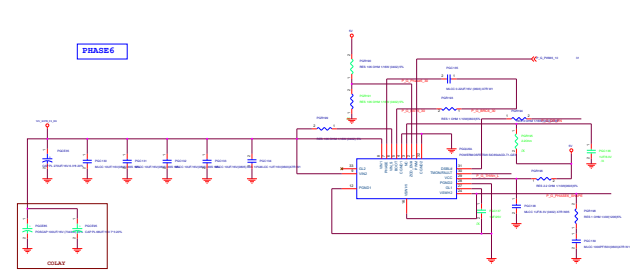
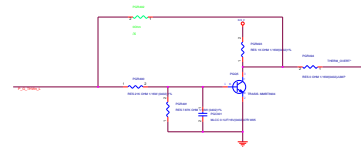
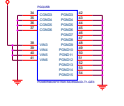
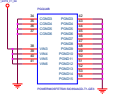
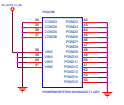
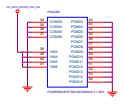
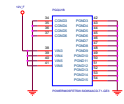
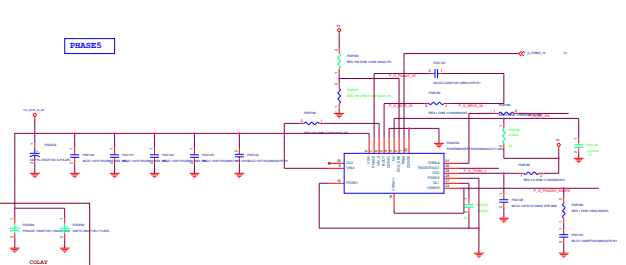
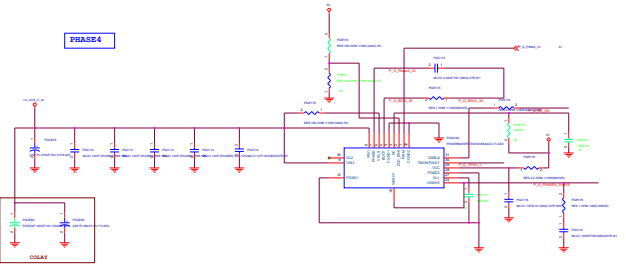
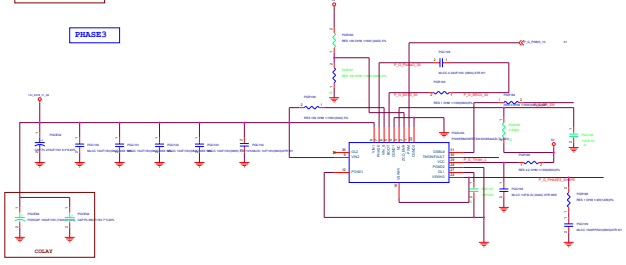
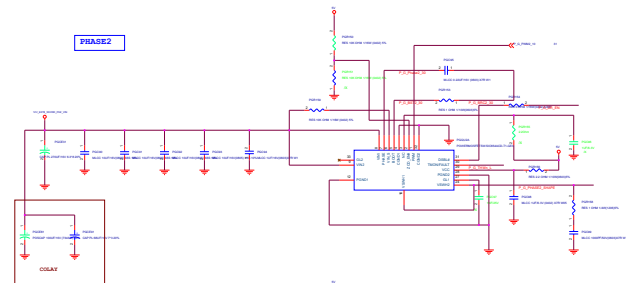
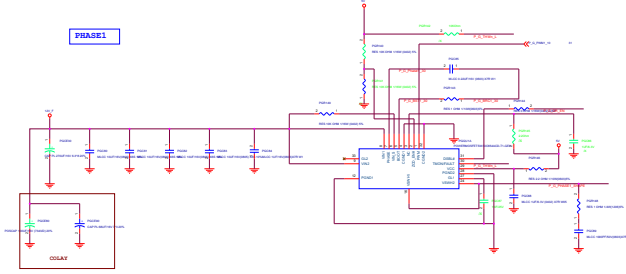
GPU02_LOW_TEMP	GPU SPEED
0	Slow
1	Normal

Title :		Hot Unplug Detect	
<OrigName>		Engineer:	
Size Custom	Project Name CG132P	Part 1.01	
Date: Wednesday, July 15, 2020	Sheet	66	of 80

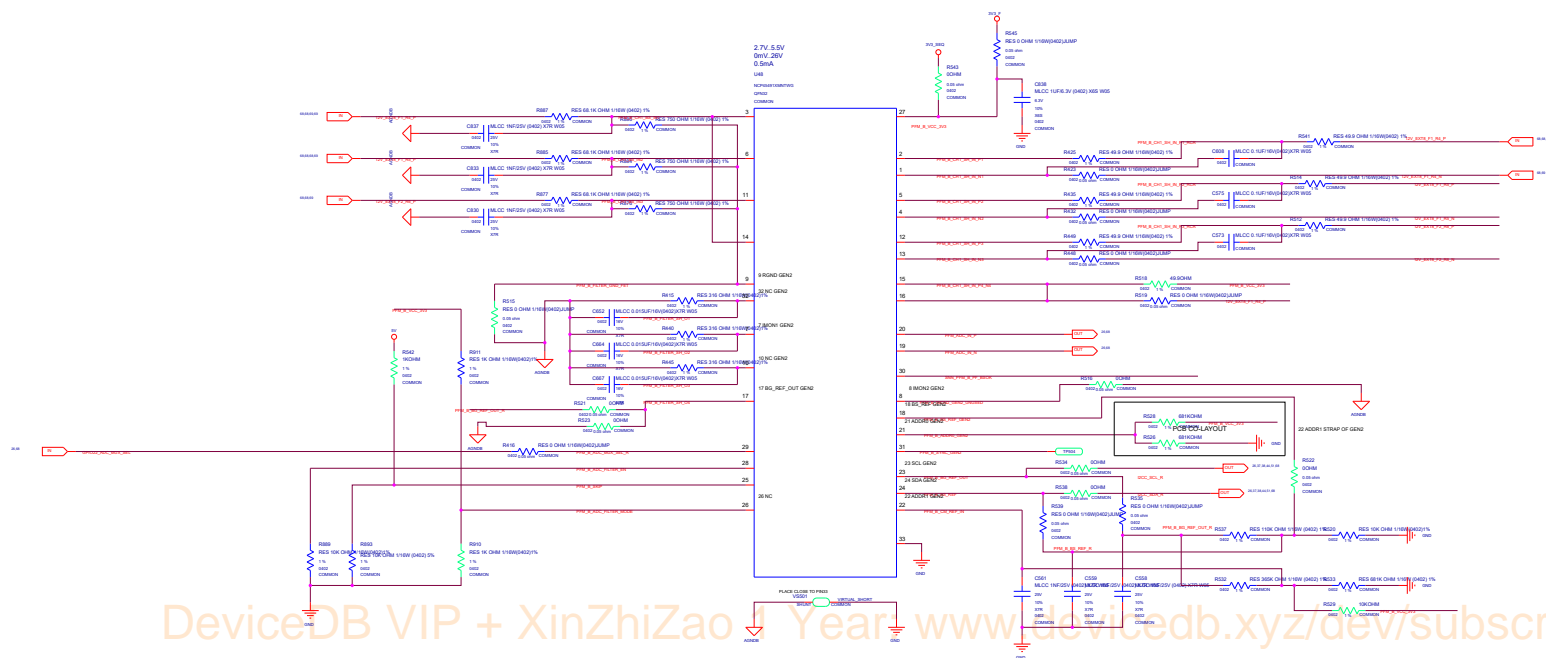
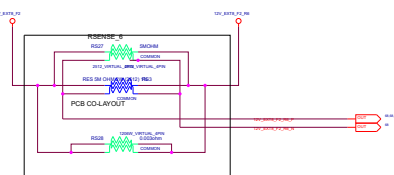
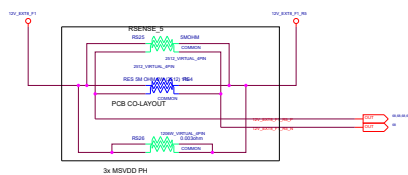
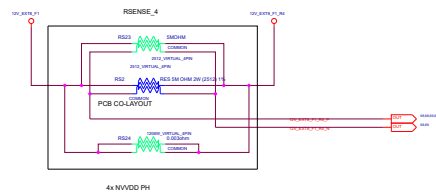
PS: Discrete Steering

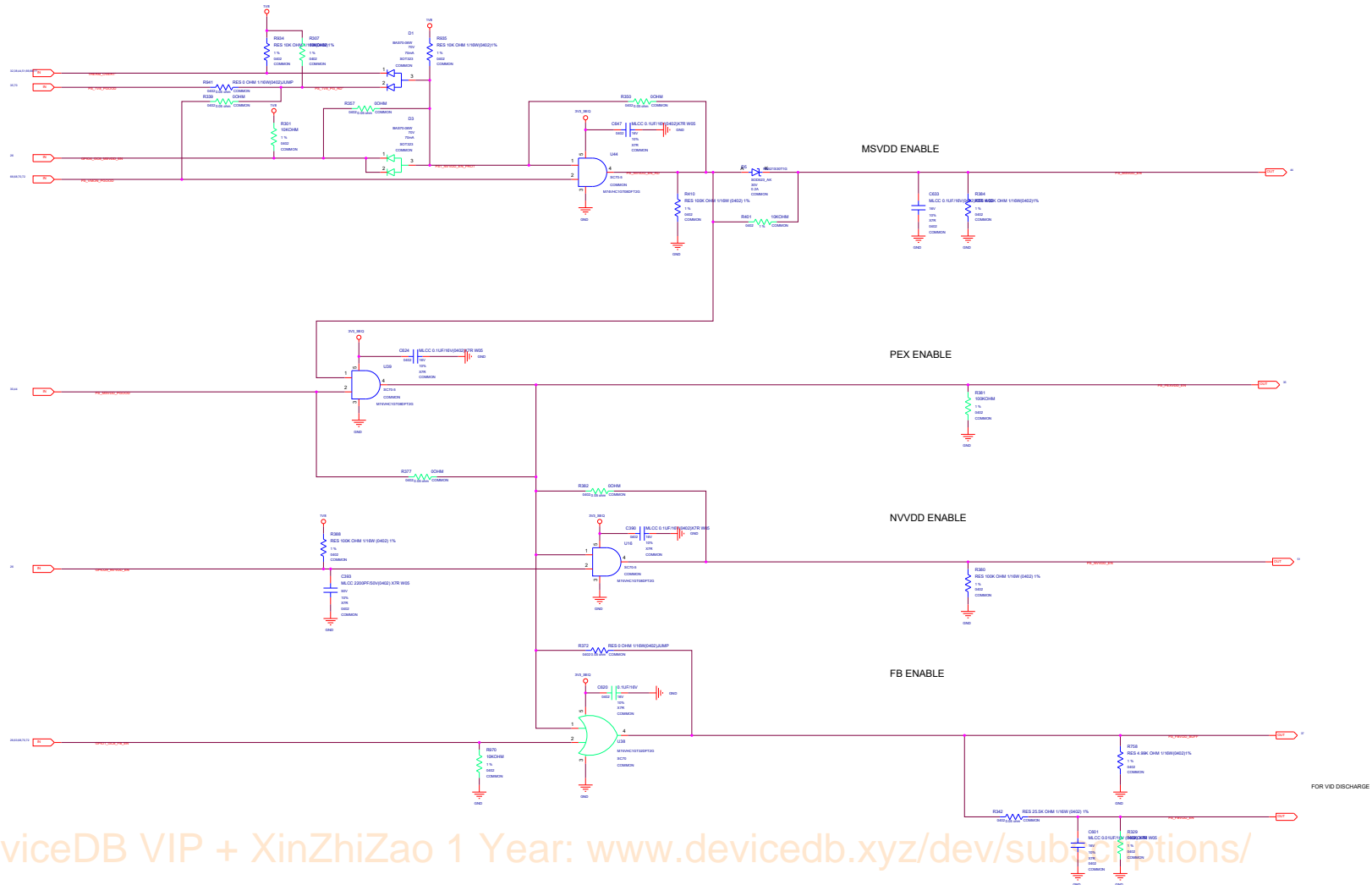
Remove PS: Discrete Steering

Title :		Steering	
Engineer:		[REDACTED]	
Size	Project Name	Rev	
Customs	CG132P	1.01X	
Date	Wednesday, July 15, 2025	Sheet	57 of 80



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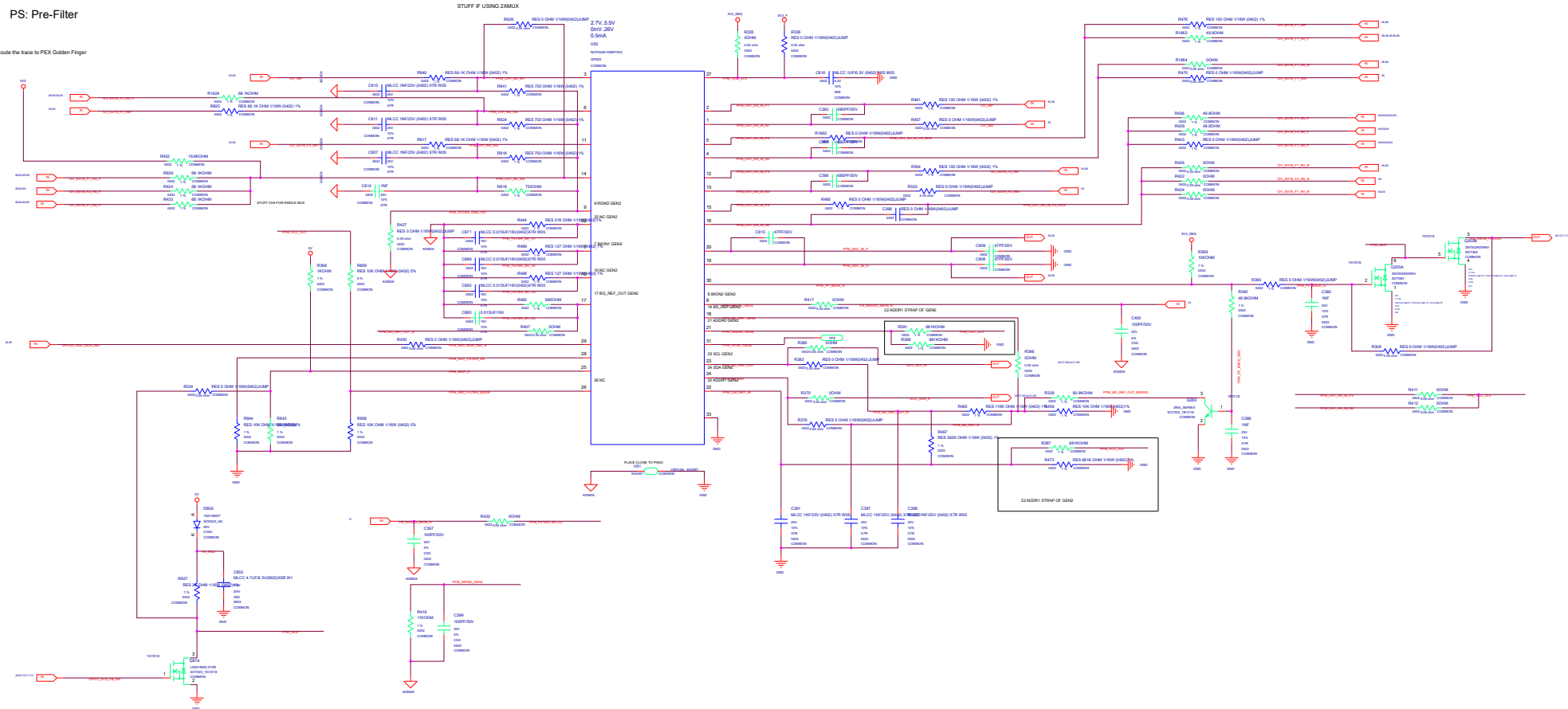


DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

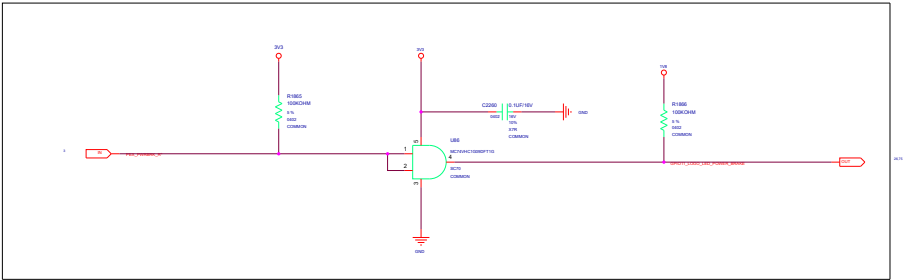
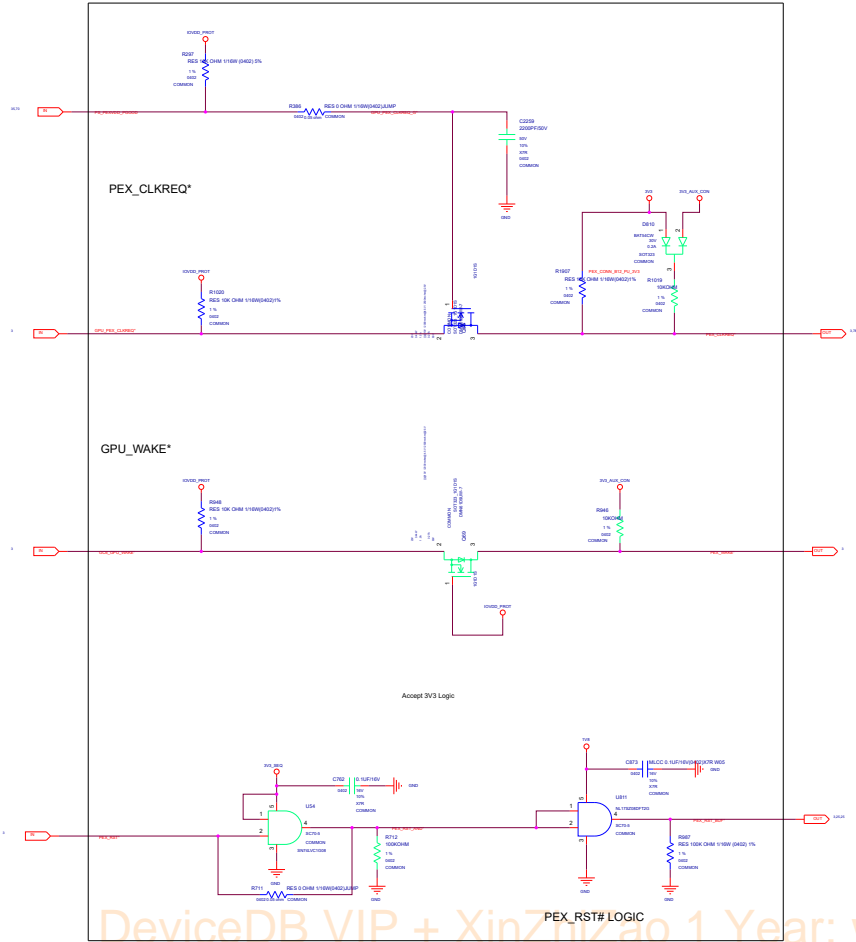
Title :		3V3 MONITOR	
-<OrgName>		Engineer: [REDACTED]	
Size	Project Name	Rev	
A	CG132P	1.01X	
Date	Wednesday, July 15, 2020	Sheet	72 of 80

PS: Pre-Filter

Route the trace to PEX Golden Finger



Title :		Pre-Filter	
<OrigName>		Engineer: [REDACTED]	
Size Custom	Project Name CG132P	Rev 1.01	
Date: Wednesday, July 15, 2003		Email: [REDACTED] @ [REDACTED] . [REDACTED]	



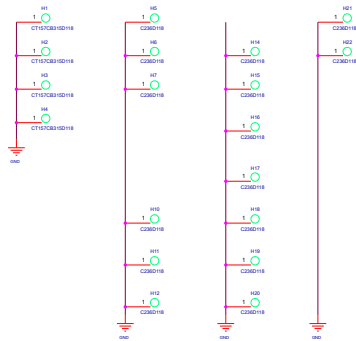
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

MISC: RGBW LED REF

Remove MISC: RGBW LED REF

DeviceDB VIP + XinZhiZao 1 Year: www.devicedb.xyz/dev/subscriptions/

Title : MISC: RGBW LED REF	
Engineer: [REDACTED]	
Drawn	Project Name
CG132P	
Date	Project
2024/05/15 10:00	15 00

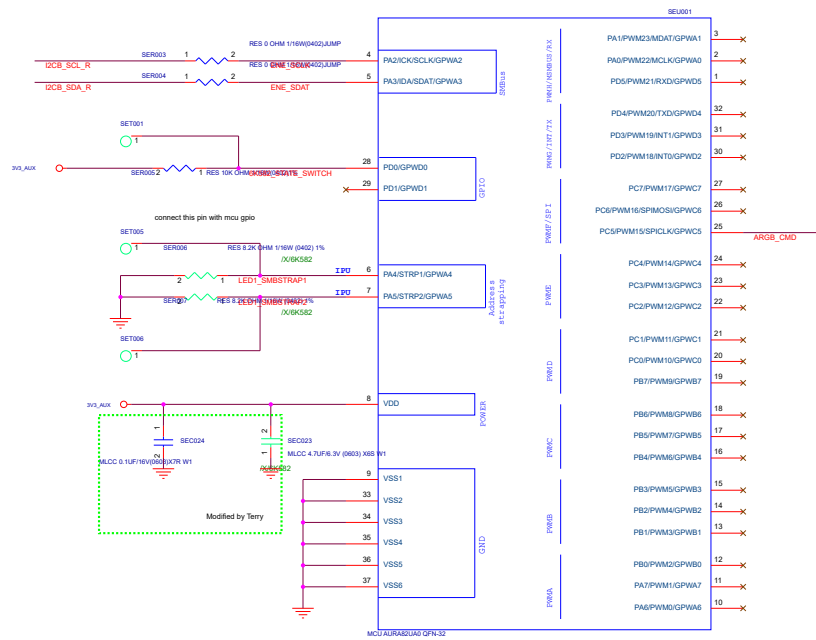


DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

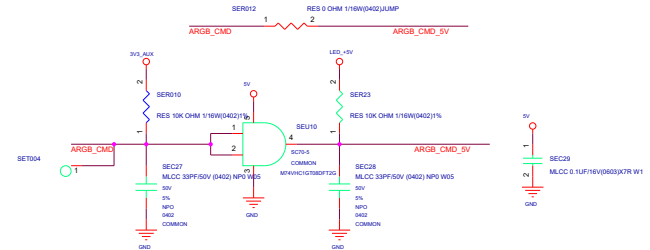
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/



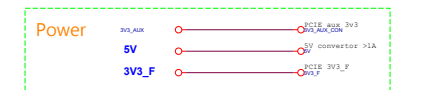
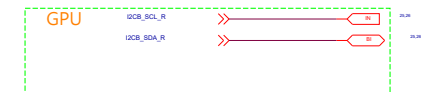
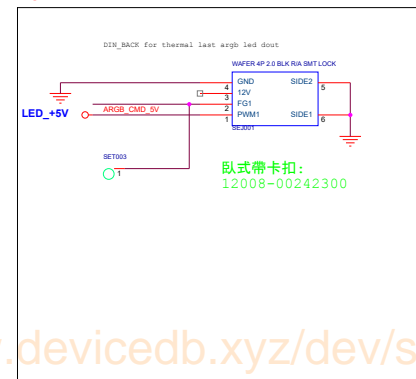
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/



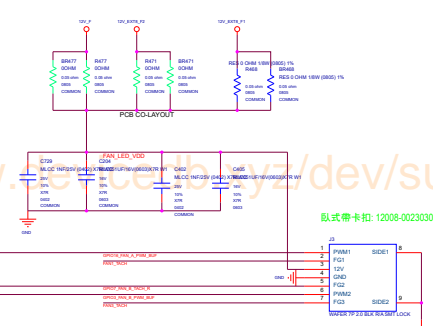
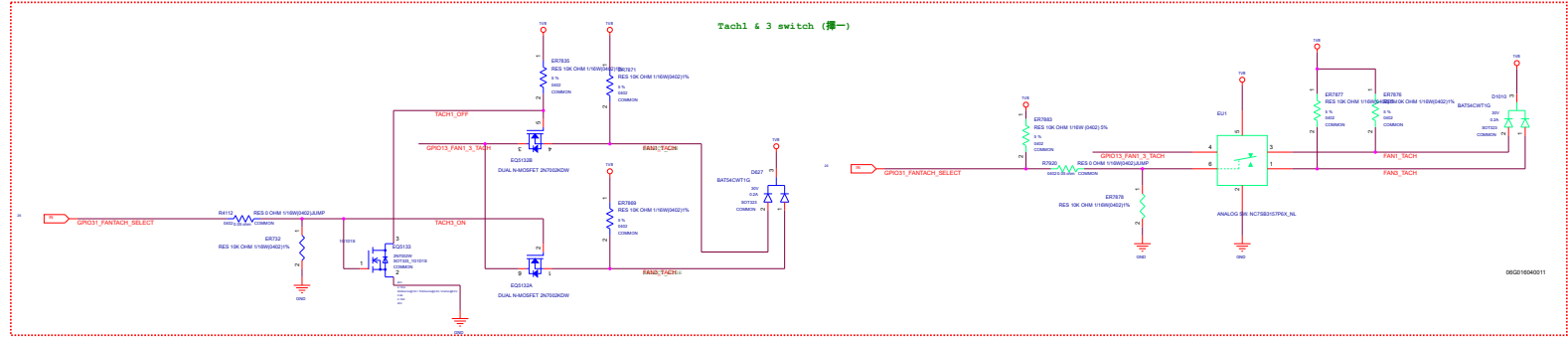
cmd 3v3->5v level shift



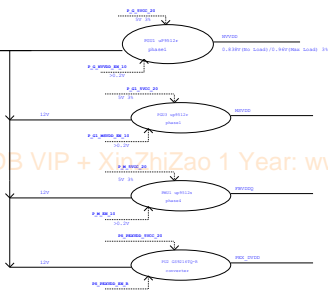
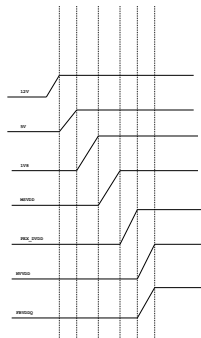
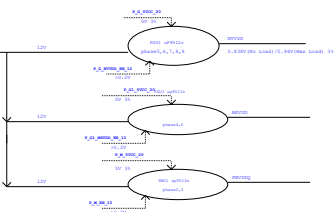
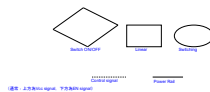
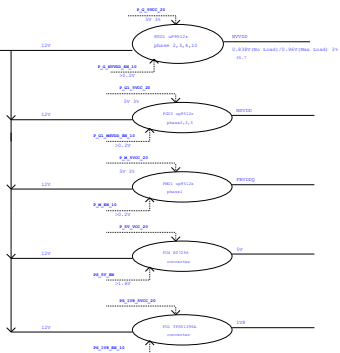
argb connector



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Title :		MISC: LED & FAN	
<OrigName>		Engineer: [REDACTED]	
State Custom	Project Name CG132P	Rev 1.01X	
Date: Wednesday, July 15, 2003	Drawn: [REDACTED]	By: [REDACTED]	By: [REDACTED]



Title :		Power Flow
Engineer:		
Rev:	CGI 32P	Rev: